REMARKS

Reconsideration of the above-identified Application is respectfully requested. Claims 1-23 are in the case. Claims 1, 7, 8, 10, 16 and 22 have been amended. Claim 23 has been added.

Regarding the objection to the claims on the grounds of alleged informalities, Claims 8 and 16 have been amended in accordance with the Examiner's kind suggestions, and therefore it is respectfully submitted that the alleged informalities have been corrected and the objection has been overcome. Wherefore reconsideration and withdrawal of this objection are respectfully requested.

Regarding the rejection of Claims 1, 7, 8, 10, 16 and 22 under 35 U.S.C. § 112, 2nd paragraph, as allegedly being indefinite, all of the alleged instances of language having the alleged indefiniteness set forth in connection with this rejection have been amended to render them definite, and it is respectfully submitted that the rejection has been overcome. In connection with this, Applicant points out for the record that in the case of Claim 10, where the word, "substantially" was deleted, Applicant has not thereby restricted the scope of the claim to only those cases where the N phases are precisely evenly spaced, and that the claim scope encompasses embodiments where the N phases may vary from the ideal in their spacing because of normal real-world variants, for example in circuit elements. Also, in order to render Claim 22 clearer, the second of two conditional limitations was deleted, and new Claim 23 was added to cover the conditional limitation deleted from Claim 22. Wherefore reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 1-7 and 14-22 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Maddux in view of Millar, this rejection is respectfully traversed in part, with Claim 1 having been amended to overcome the rejection with respect thereto and with respect to Claims 2-7, which depend, directly or indirectly, from Claim 1. Claim 1 now recites, in pertinent part, "a continuously operating blocking component that selectively blocks clock phases

which were selected for a prior transition that would erroneously contribute to a final recovered clock if not blocked, while allowing clock phases which were selected for a prior transition and that do not erroneously contribute to the final recovered clock." It was admitted that Maddux does not teach a blocking component. Millar only discloses blocking his jitter filter for start-up, to allow his system to establish lock. Thereafter, his jitter filter operates continuously. There is no teaching or suggestion in any of the art of record to modify Millar's disclosed technique for continuous operation for any purpose. It is therefore respectfully submitted that for the above reasons Claim1 is allowable over Maddux, Millar and, indeed, all of the art of record, whether considered individually or in any combination. Claims 2-7 all depend from Claim 1 and so are allowable as well for the same reasons, as well as for the additional limitations found therein.

Claim 14 recites, in pertinent part, "A clock recovery system comprising: a number of phase components that respectively obtain data samples of an NRZI encoded serial data stream, identify transitions, set a toggle bit per transition, select a clock phase based on a prior phase toggle setting, use the preceding toggle to block the current clock phase, and generate a clock…." Again, it was admitted that Maddux does not teach a blocking component. Millar only teaches a complete block of his jitter filter during start-up until lock is established. There is no teaching or suggestion of using a preceding toggle to block a current phase. The other art of record is even less relevant. It is therefore respectfully submitted that for the above reasons Claim14 is allowable over Maddux, Millar and, indeed, all of the art of record, whether considered individually or in any combination. Claims 15-17 all depend, directly or indirectly, from Claim 14 and so are allowable as well for the same reasons, as well as for the additional limitations found therein.

Claim 18 recites, in pertinent part, "setting a toggle phase according to a first identified transition of a current bit time; blocking one subsequent phase from being selected as a clock; and selecting a clock phase according to the toggle phase." Again, it was admitted that Maddux does not teach a blocking

component. Millar only teaches a complete block of his jitter filter during start-up until lock is established. There is no teaching or suggestion of setting a toggle phase according to a first identified transition of a current bit time; blocking one subsequent phase from being selected as a clock. The other art of record is even less relevant. It is therefore respectfully submitted that for the above reasons Claim 18 is allowable over Maddux, Millar and, indeed, all of the art of record, whether considered individually or in any combination. Claims 19-22 all depend from Claim 18 and so are allowable as well for the same reasons, as well as for the additional limitations found therein.

Wherefore reconsideration and withdrawal of this rejection are respectfully requested.

Regarding the rejection of Claims 8-13 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Maddux in view of Mukherjee et al., Claim 8 has been amended to overcome the rejection. Claim 8 now recites a clock and data recovery system, and sets forth, in pertinent part, "a clock recovery component that identifies transitions in the received serial data stream, selects a clock phase from a first identified transition of a bit time, blocks one other *stale* selected clock phase, and selects an *appropriate* clock accordingly" (emphasis added). For example, the Specification sets forth, at page 9, line 26 - page 10, line 2, "The blocking component 403 receives the stage 1 results from the transition analysis component and uses each of them to block a single stale clock phase selection possible for that toggle. Each clock phase selection is associated with an identified transition. The select clock component 404 then selects an appropriate clock phase, which should fall between the shortest and longest jittered bit times." It was admitted that Maddux does not teach a select clock for selecting a clock phase and generates a selected clock. By contrast with Claim 8 as presently constituted, Mukherjee et al. merely teaches a direct clock phase selection based on a weighted averaging algorithm. Thus, to the extent that the non-selected phases are argued to be "blocked," they are "fresh" with the selected clock phase, and not stale.

The other art of record is even less relevant. It is therefore respectfully submitted that for the above reasons Claim 8, as amended, is allowable over Maddux, Mukherjee et al. and, indeed, all of the art of record, whether considered individually or in any combination. Claims 9-13 all depend, either directly or indirectly, from Claim 8 and so are allowable as well for the same reasons, as well as for the additional limitations found therein. Wherefore reconsideration and withdrawal of this rejection are respectfully requested.

It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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